WHAT IS CLAIMED IS:

1. A clock system for distributing and generating a digital clock signal for a plurality of electronic assemblies, the clock system including:

a remote fixed-frequency clock for generating a first clock signal of a first frequency;

a plurality of local clock modules respectively disposed on the plurality of electronic assemblies, the local clock modules including synthesizer circuitry for creating a variable clock signal of a different frequency than the first frequency; and

fanout circuitry coupled between the remote fixed frequency clock and the plurality of local clock modules to distribute the first clock signal.

2. A clock system according to claim 1 wherein:

the synthesizer circuitry comprises a direct-digital-synthesizer having an input for receiving the clock signal of a first frequency, and a phase-locked-loop disposed at the output of the synthesizer.

3. A clock system according to claim 1 and further including:

control circuitry for generating a sync signal, the sync signal being associated with a predetermined edge from the first clock, the fanout circuitry including parallel connections for distributing the sync signal with the first clock signal; and

the local clock modules including synchronization circuitry for aligning and starting the local clock modules synchronously, based on the clock edge associated with the sync signal.

4. A clock system according to claim 2 wherein:

the synthesizer and the phase-locked-loop cooperate to generate a clock signal of a second frequency greater than the first frequency.

5. A clock system according to claim 1 wherein:

the plurality of electronic assemblies include respective pattern generators having clock inputs tied to the outputs of the respective clock modules.

6. A clock system according to claim 5 wherein:

at least two of the clock modules generate local clocks of different frequencies for the respective pattern generators.

7. A clock system according to claim 6 and further including:

coincidence point detection circuitry for determining synchronous operation between the respective pattern generators.

8. A frequency-based semiconductor tester including:

a computer workstation;

a testhead having remote fixed-frequency clocking circuitry for creating a high-accuracy clock signal of a first frequency, the testhead coupled to the computer workstation and further including a plurality of channel cards, each of the channel cards including synthesizer circuitry for creating a local frequency-based variable clock signal of a higher frequency than the first frequency; and

fanout circuitry disposed between the channel card synthesizer circuitry and the fixed frequency clocking circuitry for distributing the high-accuracy clock signal as a reference signal for the synthesizer circuitry.

9. A frequency-based semiconductor tester acccording to claim 8 wherein:

the synthesizer circuitry comprises a direct-digital-synthesizer having an input for receiving the clock signal of a first frequency, and a phase-locked-loop disposed at the output of the synthesizer.

10. A clock system according to claim 8 and further including:

control circuitry for generating a sync signal, the sync signal being associated with a predetermined edge from the first clock, the fanout circuitry including parallel connections for distributing the sync signal with the first clock signal; and

the local clock modules including synchronization circuitry for aligning and starting the local clock modules synchronously, based on the clock edge associated with the sync signal.

11. A clock system according to claim 9 wherein:

the synthesizer and the phase-locked-loop cooperate to generate a clock signal of a second frequency greater than the first frequency.

12. A clock system according to claim 8 wherein:

the plurality of electronic assemblies include respective pattern generators having clock inputs tied to the outputs of the respective clock modules.

13. A clock system according to claim 12 wherein:

at least two of the clock modules generate local clocks of different frequencies for the respective pattern generators.

14. A clock system according to claim 13 and further including:

coincidence point detection circuitry for determining synchronous operation between the respective pattern generators.

15. A method of clocking a plurality of electronic assemblies, the method including the steps of:

remotely establishing a fixed clock signal of a first frequency;

fanning-out the fixed clock signal to the plurality of electronic assemblies; and

synthesizing the fixed clock signal on the plurality of electronic assemblies to locally create a higher frequency clock signal for each of the electronic assemblies.

16. A method of starting a plurality of ATE pattern generators synchronously, the pattern generators disposed on respective channel cards, the method including the steps of:

creating a remote fixed-frequency clock;

generating a control sync signal, the sync signal associated with a predetermined edge of the fixed-frequency clock;

fanning out the fixed-frequency clock and the sync signal to a plurality of clock modules residing on the respective channel cards, the clock modules including clock synthesizer circuitry and edge prediction logic;

locally synthesizing a variable-frequency clock on each of the channel cards with the respective clock module synthesizer circuitry, the variable frequency clock of a different frequency than the fixed-frequency clock; and

passing the sync signal with the edge prediction circuitry through the first clock domain to the second variable-frequency clock domain to identify an accurate and common start time for the plurality of pattern generators.

17. A method of starting a plurality of ATE pattern generators according to claim 16 wherein at least two of the pattern generators operate at different frequencies and receive different variable-frequency clock signals from the respective clock modules, the method further including the steps of:

detecting coincidence points between the different variable-frequency clock signals; and

utilizing the detected coincidence points to identify starting times for the plurality of pattern generators.

18. A method of starting a plurality of ATE pattern generators synchronously according to claim 16, wherein the clock module synthesizer circuitry includes a plurality of direct-digital-synthesizers, and the step of locally synthesizing further includes the step of:

aligning the direct-digital-synthesizers.